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High-energy (MeV) Al and B ion implantations into 4H-SiC and fabrication of pin diodes

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High-energy (MeV) implantation of Al^+ or B^+ into 4H-SiC epilayers has been investigated. A 3 μm deep pn junction was formed by multiple-step Al^+ or B^+ implantation with implantation energies up to 6.2 or 3.4 MeV, respectively. Rutherford backscattering channeling and cross-sectional transmission electron microscopy analyses have revealed residual damages in the implanted layers even after high-temperature annealing at 1600–1800 °C. Nevertheless, high electrical activation ratios over 90% have been achieved for both Al^+- and B^+-implanted layers by annealing at 1800 °C. Mesa pin diodes with a 15-μm-thick *i* layer formed by MeV implantation have exhibited high breakdown voltages of 2860–3080 V. The reverse characteristics of diodes have been substantially improved by increasing annealing temperature up to 1800 °C. The diode performance is discussed with the results of deep level analyses near the junctions. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1459096]

I. INTRODUCTION

Through recent progress in silicon carbide (SiC) crystal growth and device processing technologies, prototype SiC electronic devices have been demonstrated, showing promise in high-power, high-frequency, and high-temperature applications.[1] To realize several kilovolts (or higher) SiC power devices such as double-implanted metal–oxide–semiconductor field effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs), deep *p*-well (*p*-base) regions are required to prevent ''punchthrough'' breakdown and to minimize the electric field crowding at the corners of the *p* well. For this purpose, high-energy implantation of acceptor ions is the most promising approach because the extremely low diffusion coefficients of dopant impurities in SiC make the diffusion process impractical. However, only several investigations have been reported on high-energy ion implantation into SiC.[2–6] Furthermore, comparative study on the implantation of Al^+ and B^+, two major acceptor impurities, into SiC has been still limited.[3,7,8] In this article, the authors describe high-energy (MeV) Al^+ and B^+ implantations into 4H-SiC(0001) epilayers. The profile of implanted ions, lattice damages, and electrical activation are discussed. Fabrication of high-voltage pin diodes is also presented.

II. EXPERIMENT

Samples used in this study were *n*-type 4H-SiC epilayers grown by chemical vapor deposition (CVD) on 8° off-axis 4H-SiC(0001) substrates in the authors' group.[9] The 10–18-μm-thick epilayers were intentionally doped with nitrogen to $0.7–2\times10^{15}$ cm^{-3}. Box profiles with a 3 μm depth were formed by multiple high-energy Al^+ or B^+ implantation into 4H-SiC epilayers. The maximum implant energies required for 3 μm deep junctions were 6.2 MeV for Al^+ and 3.4 MeV for B^+ implantations. The implantation profiles were simulated with a TRIM code,[10] and were confirmed by secondary ion mass spectroscopy (SIMS) measurements.[4] The total implant dose was adjusted to 3×10^{14} cm^{-2}, leading to an average implanted-impurity concentration of 1×10^{18} cm^{-3}. All the implantations were performed without intentional heating. Implanted samples were annealed at 1500–1800 °C for 30 min in pure Ar ambience. For the annealing at temperatures up to 1600 °C, a horizontal CVD reactor[9] was used, while a vertical hot-wall CVD reactor[11] was employed for high-temperature annealing at 1700 and 1800 °C. Samples were placed on a SiC-coated susceptor during the annealing. Neither a cap layer nor the supply of a SiH_4 gas was used.

Depth profiles of implanted atoms were determined by SIMS measurements with 8 keV O^+ as a primary beam. Implantation-induced damages were monitored by Rutherford backscattering spectroscopy (RBS) channeling measurements and cross-sectional transmission electron microscopy (TEM). The RBS spectra were acquired with a 2.0 MeV He^{2+} probing beam and a scattering angle of 170°. In capacitance–voltage ($C–V$) measurements, a double-Schottky structure with two Ni contacts on the front surface, which are 360 and 1600 μm in diameter, was employed. Detailed process conditions of pin diode fabrication are given in the Sec. III C.

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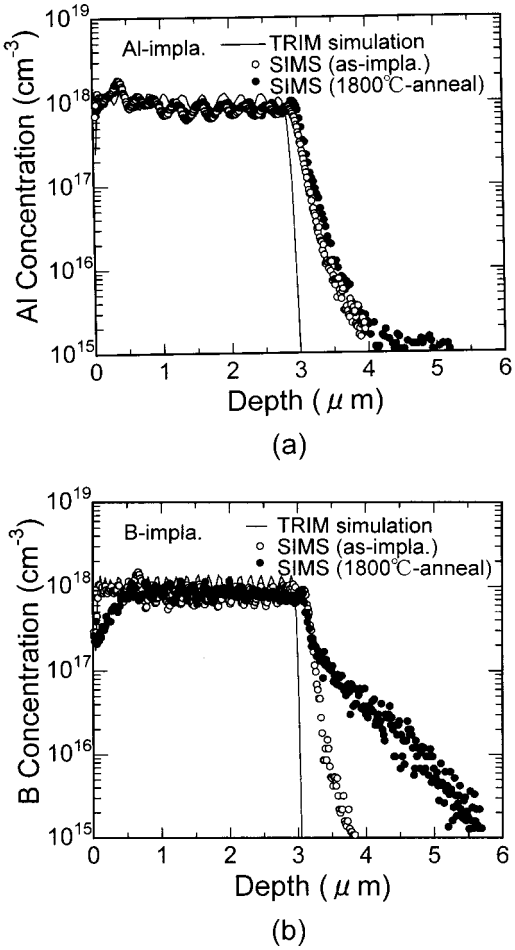

FIG. 1. Profiles of implanted atoms before and after annealing at 1800 °C for (a) Al^+- and (b) B^+-implanted SiC, indicating that 3 μm deep box profiles are formed in both cases.

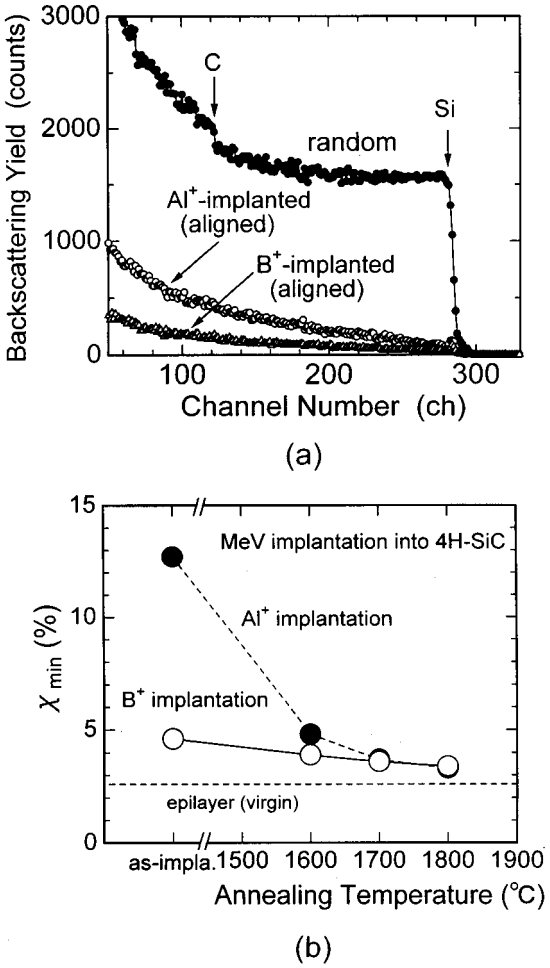

FIG. 2. (a) RBS channeling spectra of Al^+- and B^+-implanted samples without annealing (as-implanted). (b) Annealing temperature dependence of normalized backscattering yield χ_{min} for Al^+- and B^+-implanted SiC, which reflects the amount of displaced Si atoms in the region from the surface down to about 1 μm depth.

III. RESULTS AND DISCUSSION

A. Implantation profile and lattice damage

Figure 1 shows the profiles of implanted atoms before and after annealing at 1800 °C for (a) Al^+- and (b) B^+-implanted samples, indicating that 3 μm deep box profiles are formed in both cases. Although Al atoms do not diffuse even after the high-temperature annealing, significant diffusion was clearly observed for the B profile after annealing, in qualitative agreement with a previous report.[3] The B concentration near the surface region is decreased due to outdiffusion, and a long tail of B profile in the several micron-deep region, caused by indiffusion, is revealed. However, more than 90% portion of implanted B atoms still remain in SiC after this very high-temperature annealing. The diffusion of B was small after annealing at 1600 °C, and became remarkable when samples were annealed at 1700 °C or higher (not shown in Fig. 1).

Figure 2(a) represents the RBS channeling spectra of Al^+- and B^+-implanted samples without annealing (as-implanted). The RBS channeling measurements revealed that lattice damages of as-implanted samples are more pronounced for Al^+ implantation, compared to B^+ implantation, due to its larger mass and higher implantation energies required to form the same depth. For a quantitative analysis, the aligned backscattering yield normalized by the random yield (χ_{min}) in the channel range from 130 to 275 ch was calculated and is plotted in Fig. 2(b). This normalized backscattering yield χ_{min} reflects the amount of displaced Si atoms in the region from the surface down to about 1 μm depth. The C atoms in the SiC lattice are also displaced by ion implantation. It is, however, difficult to make a quantitative analysis of the displaced C atoms, because the RBS signals from C atoms, which appear in the lower channel numbers as indicated in Fig. 2, are overlapped by those from displaced Si atoms. As shown in Fig. 2(b), the χ_{min} value can be lowered to 3.2%–3.4% by increasing annealing temperature. However, the χ_{min} values for all the implanted and annealed samples are slightly higher than that obtained from a virgin (unimplanted) sample, suggesting residual damages.

Figure 3 represents the cross-sectional TEM images of Al^+- or B^+-implanted layers annealed at 1600 or 1800 °C. In B^+-implanted samples, dark spots are distributed throughout the implanted layers in TEM images with a density of 35–56 μm^{-2} [Figs. 3(c) and 3(d)]. The size of these dark spots is approximately 10–20 nm. Similar but more faint

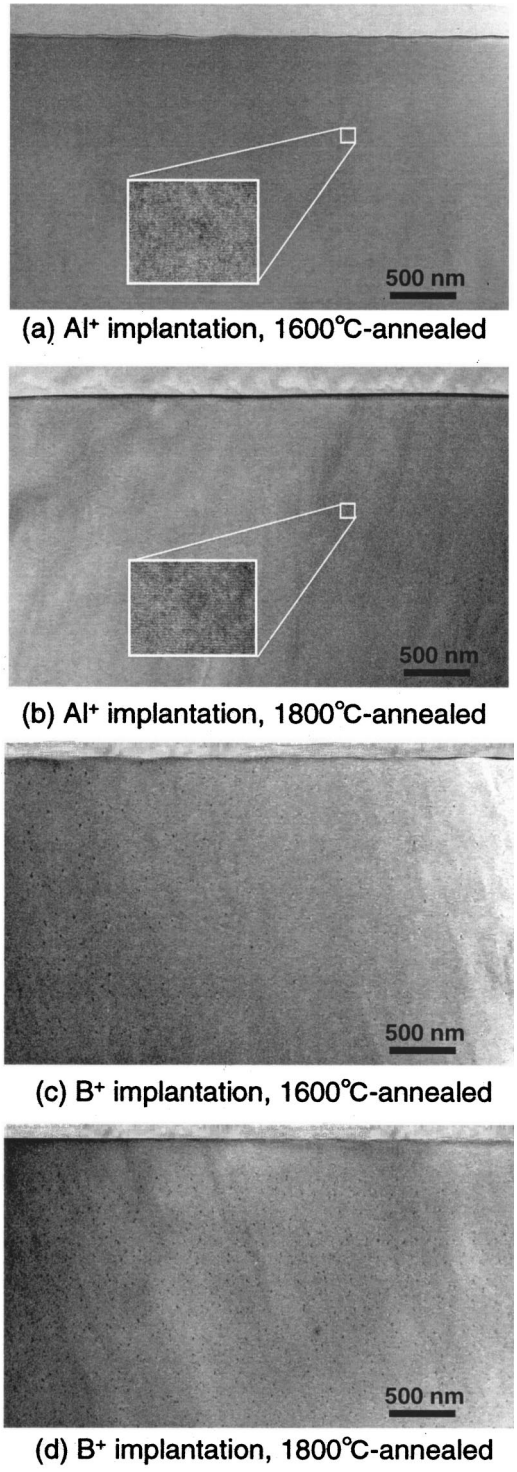

FIG. 3. Cross-sectional TEM images for Al^+- and B^+-implanted SiC layers annealed at 1600 or 1800 °C.

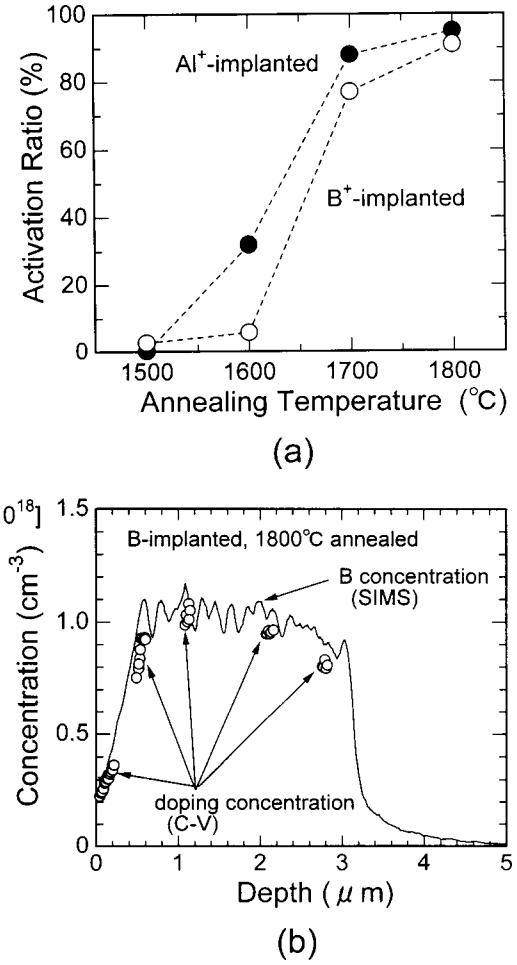

FIG. 4. (a) Annealing temperature dependence of the electrical activation ratio for Al^+- and B^+-implanted SiC layers. The closed and open circles denote the activation ratios for Al^+ and B^+ implantation, respectively. (b) Net acceptor concentrations determined by successive reactive ion etching and $C-V$ measurements for a B^+-implanted 4H-SiC layer annealed at 1800 °C. The profile of B atoms determined by SIMS is also shown by a solid curve.

spots with smaller sizes (<10 nm) and smaller number ($2-4\ \mu m^{-2}$) are also seen in the Al^+-implanted samples [Figs. 3(a) and 3(b)]. This type of dark spots has been reported in Al^+-implanted SiC, and has been ascribed to extrinsic stacking faults in the basal plane and associated dislocation loops.[12,13] Si and C interstitials generated by ion implantation may diffuse and form clusters in the basal plane during the annealing process. It is of interest that a higher density of dark spots was observed in B^+-implanted layers, damage of which is supposed to be less than that of Al^+-implanted layers as described in the RBS analysis. If the thickness of specimens in TEM analyses is assumed to be a typical value of 100 nm, the defect (dark spot) density can be estimated to be $\sim 10^{13}$ cm^{-3} for Al^+- and $\sim 10^{14}$ cm^{-3} for B^+-implanted layers. The higher defect density observed in B^+-implanted layers cannot be explained merely by implantation damage, and more microscopic consideration including the diffusion process of Si and C interstitials and the strain near impurity atoms will be required.

B. Electrical activation and surface analysis

The net acceptor concentration was determined from $C-V$ measurements on Ni/SiC Schottky structures. The electrical activation of implanted dopants was roughly estimated by the ratio of the net acceptor concentration (N_a) and the average implanted-atom concentration ($N_i \sim 1\times 10^{18}$ cm^{-3} when outdiffusion is not significant). Figure 4(a) depicts the annealing temperature dependence of the electrical activation ratio for Al^+- and B^+-implanted layers. The closed and open

circles denote the activation ratios for Al^+ and B^+ implantation, respectively. After the annealing at 1500 °C, the electrical activation was low, below 5% for both Al^+ and B^+ implantations. The activation ratio can be improved by increasing annealing temperature, and this trend agrees with our previous report on lower-energy Al^+ and B^+ implantations (Al^+:<720 keV, B^+:<360 keV).[8] Regarding the Al^+-implanted layers, nearly perfect activation (>90%) has been achieved after annealing at 1700 or 1800 °C. The activation ratio for B^+-implanted layers follows a similar dependence, but the activation ratio is slightly lower. The authors should point out that the acceptor concentration in B^+-implanted layers was only $3-4\times10^{17}$ cm^{-3} ("apparent" activation ratio: 30%–40%) even after annealing at 1700–1800 °C when measured on a Schottky structure formed on the front surface. It should be noted that $C-V$ measurements on Ni/SiC Schottky structures can probe only the near-surface region, especially when the activation ratio, or acceptor concentration, becomes high. As shown in Fig. 1(b), the B atom concentration in the near-surface region is lower than the designed concentration (1×10^{18} cm^{-3}) after high-temperature annealing due to the significant outdiffusion.

Then, successive reactive ion etching (RIE) and $C-V$ measurements were performed to determine the net acceptor concentration at depths of 0.5–0.7, 1.0–1.2, 2.0–2.2, and 2.8–3.0 μm from the surface. The net acceptor concentrations measured at these depths are plotted in Fig. 4(b), together with the profile of B atoms determined by SIMS. This experiment revealed that the net acceptor concentration in the deep region is high, $0.8-1\times10^{18}$ cm^{-3}, following the SIMS data. When the ratios of N_a/N_i were calculated at these depths, taking account of the outdiffusion, the average value reaches 91%. This value is plotted in Fig. 4(a) as the activation ratio for a B^+-implanted layer annealed at 1800 °C. It should be noted that 5%–6% of implanted B atoms was lost after the high-temperature annealing due to the outdiffusion. This loss of B atoms, however, does not affect the "total" activation ratio for the 3 μm deep profile, although the acceptor concentration near the surface is rather low. It is noteworthy that the structural defects detected as dark spots in TEM analyses do not directly affect the electrical activation of implanted impurities, because the defect density showed very little dependence on annealing temperature as in Figs. 3(c) and 3(d). Itoh *et al.* have reported that C^+ coimplantation enhances the electrical activation in Al^+ and B^+ implantations into SiC.[14] In fact, the authors observed the improvement of activation by C^+ coimplantation when annealing was done at 1600 °C. [4] However, preliminary investigation in the authors' group indicates that the effect of C^+ coimplantation, with the same C^+ implant dose as dopants, becomes negligibly small for samples annealed at 1700 °C or higher temperature.

Surface degradation is one of the key issues for implanted SiC layers after high-temperature annealing.[15,16] Figure 5 shows the Nomarski micrographs and atomic force microscopy (AFM) images for Al^+-implanted samples before and after annealing at 1800 °C. Although the surface roughness increased from 0.32 to 2.90 nm by high-temperature annealing at 1800 °C, the surface is still specular and no macrosteps are observable in both pictures. Table I summarizes the surface roughness defined by the rms for implanted SiC layers, together with as-grown samples. No significant differences were observed between Al^+- and B^+-implanted SiC layers.

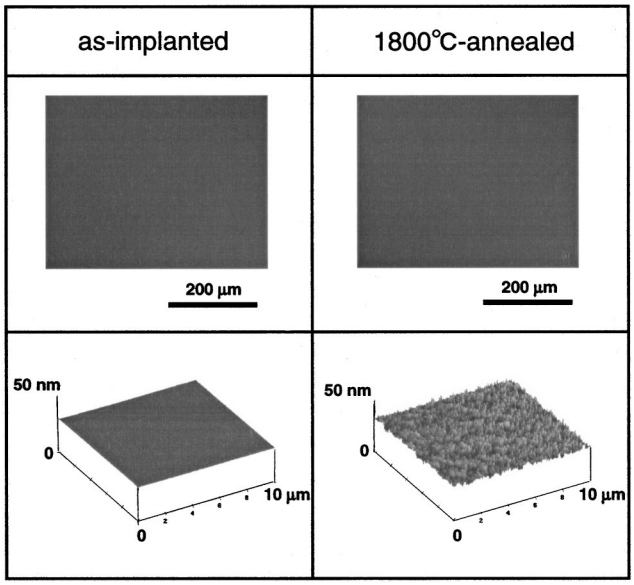

FIG. 5. Nomarski micrographs and AFM images for Al^+-implanted samples before and after annealing at 1800 °C.

The x-ray photoelectron spectroscopy (XPS) analyses were performed on these samples with the Mg $K\alpha$ line (1254.6 eV) as an x-ray source. The samples were cleaned by a Radio Corporation of America (RCA) method followed by a HF dip before loading into the XPS system. Before the measurements, the surface was subjected to a low-energy (2 keV) Ar^+ beam for 20 s to remove carbon contaminants from atmosphere. The XPS signals exhibited sharp single peaks due to sp^3 -orbital Si and C atoms in SiC, for example, a Si_{2p} peak at 100.4 eV and a C_{1s} peak at 283.3 eV. The peak height and full width at half maximum were almost identical to those measured on as-grown epilayers, indicating that no preferential evaporation of Si and no graphitization take place during the high-temperature annealing. Although the present result is somewhat contradictory to works reported by other groups,[15,16] the authors speculate that a negligibly small temperature gradient in the vertical hot-wall CVD reactor used in this study and unintentional overpressure from

TABLE I. Surface roughness (rms) for implanted and annealed 4H-SiC layers. The scan area in AFM analyses is 10 μm×10 μm.

Sample	Al^+-implanted (nm)	B^+-implanted (nm)
As-implanted	0.32	0.33
1600 °C-annealed	1.43	1.39
1700 °C-annealed	2.23	2.21
1800 °C-annealed	2.90	2.92
As-grown	0.18	0.19

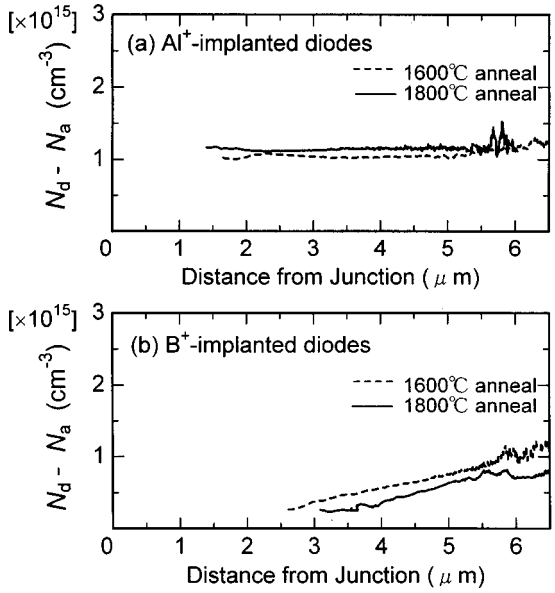

FIG. 6. Profiles of net doping concentration near the junction determined from $C-V$ measurements on (a) Al^+- and (b) B^+-implanted 4H-SiC diodes annealed at 1600 or 1800 °C.

SiC films coated on a graphite susceptor may prevent surface degradation.

C. Fabrication of pin diodes

To investigate the junction characteristics formed by high-energy implantation, mesa pin diodes were fabricated and tested. The starting materials were 13–18-μm-thick n-type 4H-SiC(0001) epilayers doped with nitrogen to 1×10^{15} cm^{-3}. The same implantation schedule as that described above was employed to create 3 μm deep junctions. Diodes were processed into mesa structures by RIE with a CF_4-O_2 system, and the surface was passivated with 30-nm-thick SiO_2 formed by wet oxidation at 1150 °C. Ohmic contacts were formed by evaporation of Al/Ti and Ni for p-type and n-type SiC, respectively, followed by alloying at 800 °C. The diode size was 100–500 μm in diameter.

Figure 6 depicts the profiles of net doping concentration near the junction, which were determined from $C-V$ measurements, for (a) Al^+- and (b) B^+-implanted diodes annealed at 1600 or 1800 °C. The net donor concentration at the deeper part away from the junction interface is almost constant, $0.8-1.2\times10^{15}$ cm^{-3}. However, the net donor concentration for B^+-implanted diodes is reduced adjacent to the junction interface, creating ''graded junctions,'' which may be attributed to the compensation of N donors with implanted B acceptors or implantation-induced point defects. The width of the ''compensated'' layers and the amount of reduction in doping concentration depend on the implanted species but not very much on the annealing temperature. The width of ''compensated i layer,'' estimated from capacitance values at a forward bias of 1–2 V, was thicker for

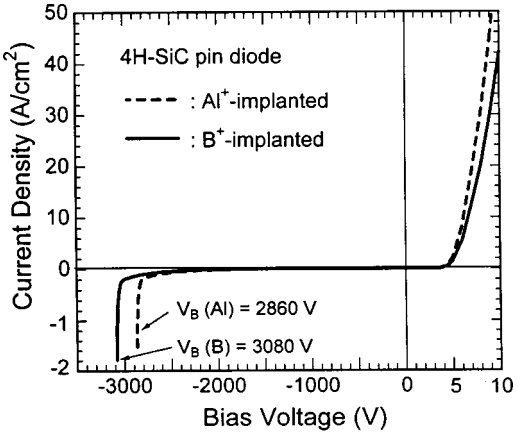

FIG. 7. Typical current density-voltage characteristics at room temperature for 100 $\mu m\phi$ Al^+- and B^+-implanted 4H-SiC pin diodes annealed at 1800 °C.

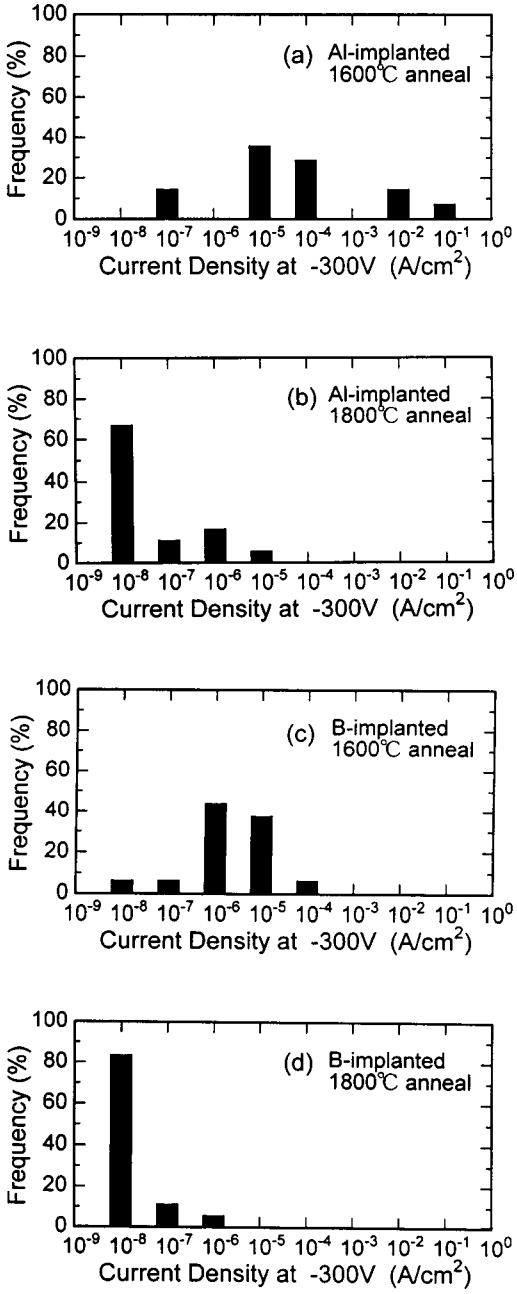

FIG. 8. Histograms of leakage current density at −300 V for Al^+- and B^+-implanted 4H-SiC pin diodes annealed at 1600 or 1800 °C.

TABLE II. Reverse characteristics of 4H-SiC pin diodes formed by MeV Al^+ and B^+ implantations.

Implanted ion	Annealing temperature (°C)	Average leakage current density at 300 V (A/cm^2)	Average breakdown voltage/ ideal breakdown voltage (%)
Al^+	1600	5×10^{-5}	39
	1800	4×10^{-8}	81
B^+	1600	2×10^{-6}	57
	1800	2×10^{-8}	90

B^+-implanted junctions (0.5–0.6 μm) than for Al^+-implanted junctions (<0.1 μm), probably due to the pronounced indiffusion of B atoms shown in Fig. 1(b).

Figure 7 demonstrates typical current density–voltage characteristics for 100 $\mu m\phi$ Al^+- and B^+-implanted diodes annealed at 1800 °C. In the forward-bias direction, the ideality factor in the low current region was close to 2.0, indicating that the recombination current is dominant. No significant differences in the forward conduction were observed among diodes fabricated in different processes (implanted species and annealing temperature). Relatively high series resistances of 72–94 $m\Omega\,cm^2$ due to nonoptimized ohmic contacts might have made it difficult to compare the forward conduction for various types of diodes. The maximum breakdown voltages achieved were 2860 and 3080 V for Al^+- and B^+-implanted diodes with 15 μm-thick n layers, respectively. Most diodes exhibited very sharp increase in reverse current at breakdown voltage, suggesting hard breakdown. The diodes could withstand relatively high avalanche current density up to 2 A/cm^2 in curve-tracer measurements. A preliminary investigation indicates that the diodes annealed at 1800 °C show more stable and nondestructive breakdown than those annealed at 1600 °C.

Considerable differences were observed in the reverse characteristics of diodes, which are critical for the blocking performance of DIMOSFETs and IGBTs. Histograms of reverse leakage currents and breakdown voltages were made through measurements on several tens of diodes for each process condition. Figure 8 shows the histograms of leakage current density at -300 V for Al^+- and B^+-implanted diodes annealed at 1600 or 1800 °C. Although the implanted-ion dependence of leakage current was small, the diodes annealed at 1800 °C exhibited much lower leakage currents with more tight distribution, compared to the diodes annealed at 1600 °C. The average leakage current densities at -300 V for four types of diodes are summarized in Table II. The average leakage current has been reduced by more than two orders of magnitude by increasing annealing temperature.

The authors have made isothermal capacitance transient spectroscopy (ICTS) measurements on these diodes.[17] Typical ICTS spectra obtained from four types of diodes at 310 K are represented in Fig. 9. Bias voltage (V_R) of 0 V and pulse voltage (V_P) of 1 V were employed in this measurement to monitor deep traps near the junction. Note that no minority carrier injection takes place under this bias condition. The analyses revealed that the major deep trap near the junction is the Z_1 center[18] with an activation energy of 0.66 eV for all the diodes. Table III shows the concentration of Z_1 center observed for four types of diodes. The trap concentration was the largest for an Al^+-implanted diode annealed at 1600 °C, being 2×10^{13} cm^{-3}, and a B^+-implanted diode annealed at 1600 °C showed one-order-of-magnitude lower trap concentration. In contrast, 1800 °C -annealed diodes exhibited extremely small trap signals, close to a noise level of the measurement system. The trap concentration could be estimated to be lower than 5×10^{11} cm^{-3} for 1800 °C -annealed diodes.[17] Thus, electrically active point defects, including the Z_1 center, might be dissociated by the high-temperature annealing. This may be the reason why the leakage current could be considerably reduced by increasing annealing temperature. It should be noted that no direct correlation between the trap concentration and the defect density revealed by TEM analyses was observed.

The average breakdown voltages divided by the ideal parallel-plane breakdown voltages, predicted from the doping concentration and n-layer thickness, are also shown in Table II. Again, it is obvious that the annealing at 1800 °C is

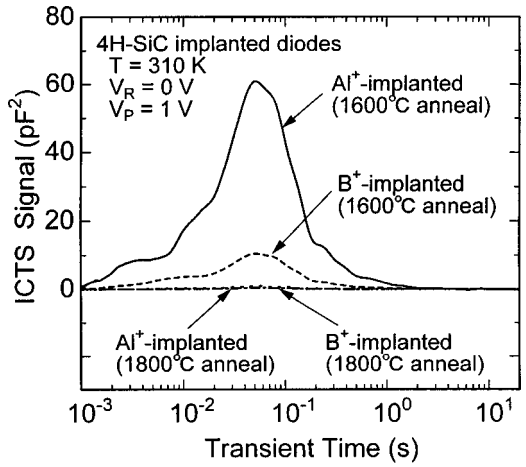

FIG. 9. Typical ICTS spectra obtained from four types of diodes at 310 K. Bias voltage (V_R) of 0 V and pulse voltage (V_P) of 1 V were employed in this measurement to monitor deep traps near the junction.

TABLE III. Z_1 center concentration observed near the junctions for MeV Al^+- and B^+-implanted 4H-SiC diodes.

Sample	Al^+-implanted (cm^{-3})	B^+-implanted (cm^{-3})
1600 °C-annealed	2×10^{13}	3×10^{12}
1800 °C-annealed	$<5\times10^{11}$	$<5\times10^{11}$

effective to improve the blocking performance of implanted diodes. More than 80% of the ideal breakdown voltage could be achieved by 1800 °C annealing. Concerning the diodes annealed at a fixed annealing temperature, B^+ implantation has resulted in higher breakdown voltages than Al^+ implantation. A similar tendency has been reported for SiC diodes formed by lower-energy Al^+ and B^+ implantation.[7,8] Although the reason for this implanted-ion dependence of diode performance is not clear at present, the indiffusion of B might give an effect on the reverse characteristics. For example, the compensated *i* layer near the junction is thicker for B^+-implanted diodes, as discussed eariler by using Fig. 6. Owing to this *i* layer, the electric field distribution near the junction may become more flat, leading to higher breakdown voltages. Besides, the authors speculate that the defects observed in TEM may give little influence on the reverse characteristics of diodes. However, more detailed characterization of both structural and point defects are required before making conclusive interpretation.

IV. CONCLUSIONS

MeV Al^+ and B^+ implantations into 4H-SiC epilayers have been investigated. The 3 μm deep box profiles were formed through multiple-step implantation with energies up to 6.2 MeV for Al^+ and 3.4 MeV for B^+ implantations. Both in- and outdiffusion were observed for the B^+-implanted samples subjected to annealing at 1700 °C or higher temperature. The lattice damages of as-implanted samples monitored by RBS channeling measurements were much smaller for B^+-implanted layers. However, B^+-implanted layers showed a higher density of structural defects, detected as dark spots in cross-sectional TEM analyses. The electrical activation ratio has been improved by increasing annealing temperature, and nearly perfect ($>$90%) activation has been achieved in both Al^+- and B^+-implanted layers by annealing at 1800 °C, where the outdiffusion must be taken into account in the case of B^+ implantation. Mesa pin diodes with 15-μm-thick *n* layers formed by MeV implantation exhibited stable and nondestructive breakdown at high reverse voltages of 2860–3080 V. The high-temperature annealing at 1800 °C has resulted in the significantly improved reverse leakage current and breakdown voltage, compared to the annealing at 1600 °C. The present study shows that MeV ion implantation is a viable technique to fabricate deep *pn* junctions, which are useful for fabrication of future high-voltage SiC devices.

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